

**AMENDMENTS TO THE SPECIFICATION:**

Please delete the word "Description" at page 1, line 1.

Please add the following centered heading at page 1, line 4:

**TECHNICAL FIELD**

Please amend line 5 as follows:

~~The present invention~~ This patent application relates to the production of field effect transistors with LDD.

Please add the following centered heading at page 1, line 6:

**BACKGROUND**

Please add the following centered heading at page 2, line 10:

**SUMMARY**

Please delete the two paragraphs on page 2, lines 11 to 15.

Please add the following centered heading at page 3, line 20:

**DESCRIPTION OF THE DRAWINGS**

Please add the following centered heading at page 4, line 9:

DETAILED DESCRIPTION

Please amend the paragraph on page 8, lines 7 to 17, as follows:

The spacers 7 need not necessarily precisely cover the sidewalls of the gate electrode and the sloping sidewalls 5 as shown in Figure 5. Instead, for example, a lower portion of the sloping sidewalls 5 and/or an upper portion of the sidewalls of the gate electrode may remain uncovered by the spacers 7. It may also be provided that the spacers 7 also cover a portion of the horizontal upper surface of the substrate 1. The diagrams shown in Figures 5 and 6 are idealized in these terms. ~~What is essential for the embodiment of~~ The spacers ~~is only that they are~~ should be sufficiently thin, at least in their lower portion, in the direction intended for implantation of the low dopant concentration to allow sufficient dopant to penetrate, and that in the direction that is perpendicular to the upper surface of the substrate, they form an adequate gate-side shielding against the high-angle source/drain implantations.

Please replace the Abstract on page 12 with the following new Abstract:

A method for producing a transistor structure with a lightly doped drain (LDD) includes structuring a gate electrode on a gate dielectric. The method also includes etching the semiconductor body or substrate to form sloping sidewalls on regions adjacent to the gate electrode, and anisotropically back-etching the spacer layer to form spacers. The gate electrode is used as a mask to implant dopant to form a source region, a drain region, and regions of lower dopant concentration. Implanting dopant is performed at a first angle relative to the upper surface of the semiconductor body or substrate to form the source and drain regions, and at a second angle relative to the upper surface of the semiconductor body or substrate, and through the spacers, to form the regions of lower dopant concentration. The first angle is greater than the second angle.

Please delete the phrase "Figure 6" at page 12, line 13.